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Analog and RF Performance Evaluation of Dual Metal Double Gate High-k Stack (DMDG-HKS) MOSFETs

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Dual Metal Gate (DMG) technology was proposed to reduce the short channel effects (SCE's) of double gate MOSFETs. But, DMG alone is not enough to rectify the problem of gate tunneling current due to thinning of oxide layer with device downscaling. So, the use of high-k dielectric as gate oxide is considered to overcome the gate tunneling effect. But, high gate dielectric thickness leads to higher fringing fields leading to undesirable higher gate capacitance. So, the use of oxide stack i.e. a combination of silicon dioxide and high-k dielectric material is preferred as gate oxide. This paper presents the evaluation of the analog performance of nMOS dual metal double gate with high-k oxide stack (DMDG-HKS) MOSFETs, comparing their performance with those exhibited by dual metal double gate (DMDG) transistors and single metal double gate (SMDG) transistors of identical dimensions. The analog performance has been investigated in subthreshold regime of operation by varying the channel length, gate oxide stack and considering different analog parameters extracted from the 2-D device simulations. It has been observed that the DMDG-HKS devices offer better transconductance g_m, early voltage V_a, intrinsic gain g_m / g_d, drain conductance g_d, transconductance generation factor g_m / I_d, transition frequency f_T, etc. The variation of these analog parameters has also been investigated by changing the equivalent oxide thickness (EOT) and channel length of the DMDG-HKS transistor and has been observed that above parameters tends to improve with channel length and EOT as well.

Keywords: Dual metal double gate high-k stack (DMDG-HKS), Analog operation, Short channel effects (SCES), High-k dielectric, Equivalent oxide thickness (EOT), Transition frequency.

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1. INTRODUCTION

The continuous scaling of MOS devices leads to increased short channel effects (SCEs) and higher leakage current due to reduced gate controllability over the channel. Double gate (DG) or multi-gate devices provide a better scalability option due to its excellent immunity to SCEs [1-3]. However, for channel lengths below 100 nm, DG MOSFETs still show considerable threshold voltage roll-off and drain induced barrier lowering (DIBL) effects. To overcome this effect, Dual Metal Gate (DMG) technology was proposed [4-6] in which two different materials with different work function are merged together to form a single gate of the bulk MOSFETs. In DMG, the work function of metal gate 1 (M1) is chosen greater than that of metal gate 2 (M2). This workfunction difference in two metal gates used introduces a potential step in the channel which suppresses SCEs and enhances transconductance and a more uniform electric field distribution along the channel [4]. Since decreasing the dimensions of the device needs simultaneous decrease of the oxide thickness. This, in turn, produces undesirable gate current due to tunneling effect. In particular, gate tunneling becomes a problem in sub 100 nm regimes which increases exponentially with decreasing gate oxide (SiO_2) thickness [7]. In order to reduce the gate tunneling current, high permittivity (high-k) dielectrics has been considered as an alternative to replace SiO_2 for gate oxide. Among the various requirements of gate oxide materials, the most important are good insulating properties and the capacitance performance. Because the gate dielectric materials constitute the interlayer in the gate stacks, they should also have the ability to prevent diffusion of dopant such as boron and phosphorous and their inherent electrical defects often compromises the breakdown performance. Many candidates of possible high-k gate dielectrics have been suggested to replace SiO_2 including nitride based oxide Si_3N_4, Hf based oxides HfO_2, and Zr based oxides ZrO_2 [8]. However, if only a single higher gate dielectric having same EOT as in (SiO_2) is used then the physical thickness of oxide layer increases resulting in higher gate fringing fields. Fringing of electric field from the source / drain junctions to channel induces lowering of the potential barrier thereby causing lower threshold voltage, worse subthreshold swing, and increased off state leakage current [9]. Therefore, the use of high-k stack (HKS) i.e. a combination of silicon dioxide and high-k dielectric material is preferable as gate oxide [10] to reduce the overall gate height. At the same time, recently the subthreshold operations of MOS transistors have gained a lot of interest for ultra low power analog applications which exploit the higher g_m / I_d [11, 12] ratio.

For realizing the dual metal (DM) gate structure different process integration approaches, like dual metal (Ti / Mo) [31], metal (Ti / Ni) inter diffusion [32], metal (Ru / Ta) alloying [33], fully silicided doped poly silicon and tunable work function metal (Mo) gate [34, 35], have been used till date. The metal gates re-

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quire chemical and thermal stability and proper work function for the gate first processing. To maintain scaled performance, it becomes necessary to identify pair of metals having work functions within ~ 0.2 eV of conduction and valence band edges. Mid-gap work function metals (TiN / W) are not suitable for MOS devices since they lead to high threshold voltage. Sputtering deposition of metal gate looks to be promising as compared to chemical vapor deposition (CVD) because the impurities contained in the CVD metal degrades the dielectric properties. But the surface damage of gate dielectric during the sputtering deposition is still a major concern [26, 27]. High-k with metal gates was first proposed for integration based upon a disruptive approach known as FUSI (Fully Silicidation of poly-silicon gate electrode) [18], but it is difficult to control the silicide phase to achieve low threshold voltage. Nowadays, there are two integrations: (1) gate first (known as MIPS, metal inserted ploy-silicon) and (2) gate last (known as RMG, replacement metal gate). Here the terms first and last refers to metal electrode deposited before/after high temperature anneal. Gate first method can modulate the threshold voltage by creating dipoles through thin capping layers of Al_2O3 for PMOS and LaO_x for NMOS [22, 23]. But thermal instabilities in HK / MG devices lead to threshold voltage shifts and regrowth in the gate stack. In the gate last process hafnium dielectric is deposited before the sacrificial gate. After high temperature Source / Drain and silicide annealing, the dummy gate is removed and metal gate electrode is deposited at last [24]. Recently UMC revealed a hybrid approach combining both gate first (for *n*-MOS) and gate last (for *p*-MOS) [25]. This process is complex and difficult to scale at lower technology nodes.

In this paper, first we investigate the influence of high-k above silicon dioxide (i.e. high-*k* / SiO_2, HKS) on DMDG MOSFETs for improved SCEs and analog performance. The analog performance parameters, namely transconductance g_m, transconductance generation factor g_m / I_d, drain conductance g_d, early voltage V_a, and intrinsic gain g_m / g_d, transition frequency f_T, are systematically investigated. The impact of high-k gate dielectrics (Si_3N_4, HfO_2) and high-k stacks (HKS) in DMDG (i.e. DMDG-HKS) MOSFETs on the device short channel and analog/RF performance has been carried out. Comparison of the same with that of DMDG without HKS and single metal double gate (SMDG) MOSFETs has shown improved short channel effects and analog performance. In the latter part of the paper the DMDG-HKS MOSFETs has been compared for their analog performance by changing the channel length and gate oxides, respectively.

2. DEVICE DESIGN AND STRUCTURE

Fig. 1 shows a 2-D cross-sectional view of a dual material double gate high-k stack (DMDG-HKS) MOSFET. The structure has been generated using the Sentaurus Structure Editor (SentaurusSE) of Sentaurus TCAD [13]. All the devices assumed are *n*-channel and simulations are performed for silicon body thickness t_{Si} of 10 nm, source / drain doping concentrations of 1×10^{20} cm^{-3}(Arsenic) and silicon body doping of 1×10^{16} cm^{-3} (Boron) for different gate lengths. The body used is lightly doped to avoid carrier mobility degradation. For single metal double gate (SMDG) MOSFETs, the gate material used is Molybdenum (M1, work function = 4.55 eV) and gate oxide (SiO_2) thickness of 2 nm. The gate oxide thickness used is 2 nm to prevent the gate tunneling current.

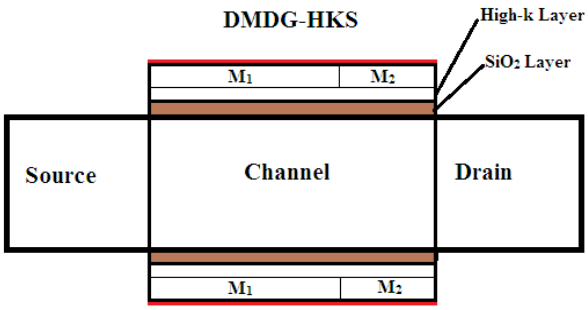


Fig. 1 – Cross -sectional view of an *n*-channel DMDG-HKS MOSFET

For DM MOSFET the device parameters used are as provided in Table 1. All parameters of DMDG-HKS are same with DM, except for the gate oxide that comprises of 1 nm thick high-k material layer on 1 nm thick SiO_2 layer. Simulations of DMDG-HKS have been carried for high-k permittivity values of 7.5 and 25 corresponding to Si_3N_4 and HfO_2, respectively. The conventional devices are simulated using the drift-diffusion transport model which assumes that the devices are always isothermal. SRH recombination model has been used to take into account for the carrier generations in space charge region and recombination in high injection regions. The doping and electric field dependent mobility models have been used in our simulations.

3. RESULTS AND DISCUSSION

In this section we discuss the results obtained through device simulations in the following order- subsection (3.1-3.3) compares DC characteristics, analog characteristics, and RF characteristics, respectively, for DMDG-HKS, DMDG and SMDG MOSFETs with different gate lengths and in subsection (3.4) we compare the analog and RF parameter variations of DMDG-HKS with respect to length.

3.1 DC Characteristics

Figs 2a and 2b show the drain current in the ON and OFF states, respectively. It is observed that the ON state current for the DMDG-HKS is higher among all structures for the physical oxide thickness of 2 nm for all the cases, since the EOT is less as compared to the DMDG or SMDG structures. This clearly shows that the gate has more control over the channel, enhancing the ON state current while reducing the OFF state current.

$$EOT = (\varepsilon_{SiO_2} / \varepsilon_{high-k}) t_{high-k} \quad (1)$$

Where ε_{SiO_2} and ε_{high-k} are relative permittivities of SiO_2 and high-k dielectric materials, respectively.

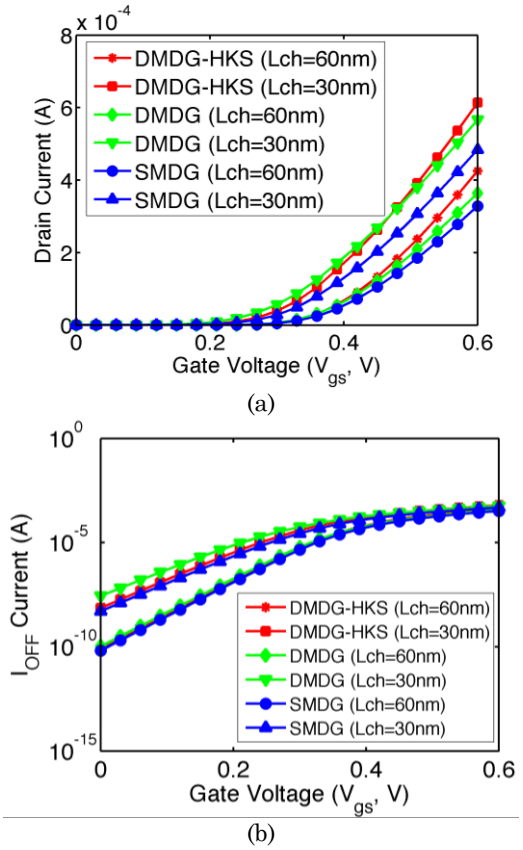


Fig. 2 – Drain current in ON state (a) and OFF state (b)

For assessing the short channel effect (SCE) behavior we extracted the values of the subthreshold slope (SS) and drain induced barrier lowering (DIBL). The SS is defined as the inverse of gate voltage required for changing the drain voltage by one decade. The DIBL is defined as the ratio of change in threshold voltage to the change in drain voltage, given by

$$DIBL = \frac{V_{TH}|_{V_{DS}=V_1} - V_{TH}|_{V_{DS}=V_2}}{V_2 - V_1} \qquad (2)$$

Where $V_{TH}|_{V_{DS}=V_1}$ and $V_{TH}|_{V_{DS}=V_2}$ are the threshold voltages at drain voltage V_1 and V_2, respectively.

The values of the threshold voltage are extracted generally for the typical values of drain voltage at 0.1 V and 1V [10].

In Table 2, the SS and DIBL for different relative permittivities of high-k layers have been compared for SMDG, DMDG, and DMDG-HKS ($K = 7.5$ of Si_3N_4 and $K = 25$ of HfO_2) MOSFETs. It can be observed that the both parameters have improved values with the use of the high-k dielectric material as gate stack. These values further improve with increment in the high-k dielectric permittivity reducing the SCEs.

Table 1 – Device parameters

Structure	Channel length (nm)		Body thickness (t_{Si} nm)	Metal gate WF* (eV)		Oxide thickness		Equivalent oxide thickness (EOT)
	M1	M2		M1	M2	SiO_2	$t_{high\text{-}k}$ ($k = 7.5$)	
DMDG-HKS $L_{ch} = 60$	45	15	10	4.55	4.10	1 nm	1 nm (HfO_2))	1.52 nm
DMDG-HKS	20	10	10	4.55	4.10	1 nm	1 nm	1.52 nm
DMDG-HKS	45	15	10	4.55	4.10	2 nm	--	2.00 nm
	20	10		4.55	4.10			
SMDG	60	--	10	4.55	--	2 nm	--	2.00

Note: *WF = Workfunction

Table 2 – SS and DIBL for different structures

Device	SS	DIBL
SMDG	66.12	9.000
DMDG	65.00	4.000
DMDG-HKS ($K = 7.5$)	64.75	2.434
DMDG-HKS ($K = 25$)	64.107	1.8233

Fig. 3 shows the variation of electric field along the direction of current flow with different work function differences (ΔWF) of the DMDG-HKS MOSFETs as shown in Table 3. As expected the largest work function difference gives rise to lowest peak electric field at the drain side. As such, it can be concluded that a larger work function difference of the two gate materials leads to a better carrier transport efficiency due to reduction in electric field at the drain side. Same conclusion can be reached for the screening effect and suppression of the SCEs and hot carrier effects (HCEs) [4].

3.2 Analog Characteristics

For analog applications, importance is emphasized to the subthreshold region of operation since power dissipation in this region is very small. Analog parameters such as transconductance (g_m), transconductance generation factor (TGF, g_m / I_d), drain conductance (g_d), early voltage (V_a) and intrinsic gain (g_m / g_d) or (g_m / I_d)×V_a have been compared between different structures with different channel lengths as shown in Table 1. The use of gate stack increases the gate control over the channel carrier due to reduction of EOT which results in better output characteristics [14].

Fig. 4 depicts the transconductance values of different structures indicating that DMDG-HKS with higher relative permittivity has the largest g_m. Another important parameter is the TGF, which is viewed as the available gain per unit value of power dissipation [15] and is shown in the Fig. 5. In the subthreshold regime,

Table 3 – DMDG-HKS MOSFETs with different workfunction difference (Fig. 3)

Structure	$L1$ (nm)	$L2$ (nm)	$M1$ WF (eV)	$M2$ WF (eV)	High-k (K)
1	45	15	4.55	4.55	25
2	45	15	4.55	4.40	25
3	45	15	4.55	4.10	25

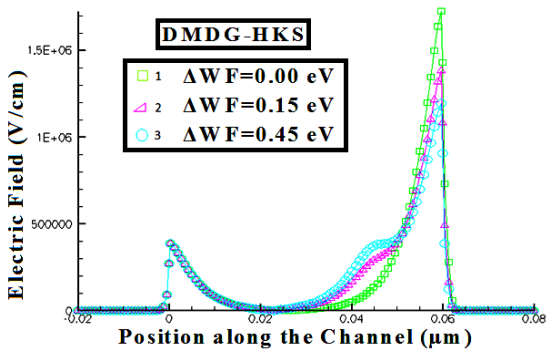


Fig. 3 – Electric field along the channel for DMDG-HKS with different workfunction difference (ΔWF) at $V_{DS} = 1$ V and $V_{GS} = 0.15$ V

TGF of DMDG-HKS with $K = 25$ is slightly higher than the remaining three structures and its value decrease while approaching towards the super-threshold regime. As seen in Fig. 5, exactly same values of SMDG and DMDG-HKS curves are obtained, which means the HKS has smaller EOT but does not scarify the TGF.

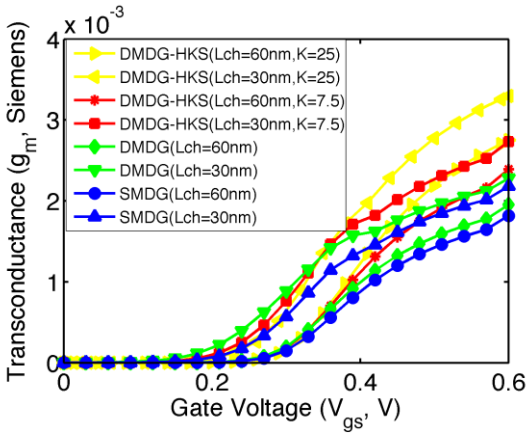


Fig. 4 – Comparison of transconductance at $V_{DS} = 0.6$ V and $V_{GS} = 0.6$ V for different structures

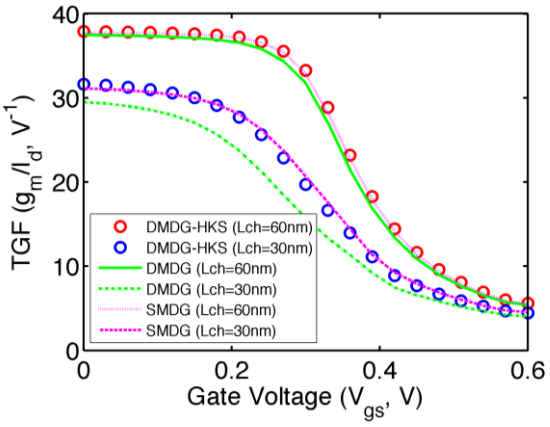


Fig. 5 – Transconductance generation factor of different structures at gate to source voltage of 0.6 V and drain voltage of 0.6 V

Fig. 6a shows the comparison of g_d as a function of gate voltage. Drain conductance g_d of Dual Metal (DM) Gate MOSFETs are lower than their Single Metal (SM) counterparts. DM Gate structures can suppress SCEs due to the screening effect, which is induced by a step change of the potential along the channel. All V_{DS} increase is dropped under gate M2 across the channel region; screening channel region under the gate M1 from drain potential variations. As a consequence, V_{DS} has only a very small influence on drain current after saturation and the g_d of DM Gate MOSFETs is very small [4]. DMDG-HKS ($K = 25$) has the least g_d both due to dual metal gate technology and increased gate controllability due to higher relative permittivity of the gate oxide stack. Similarly, the output resistance

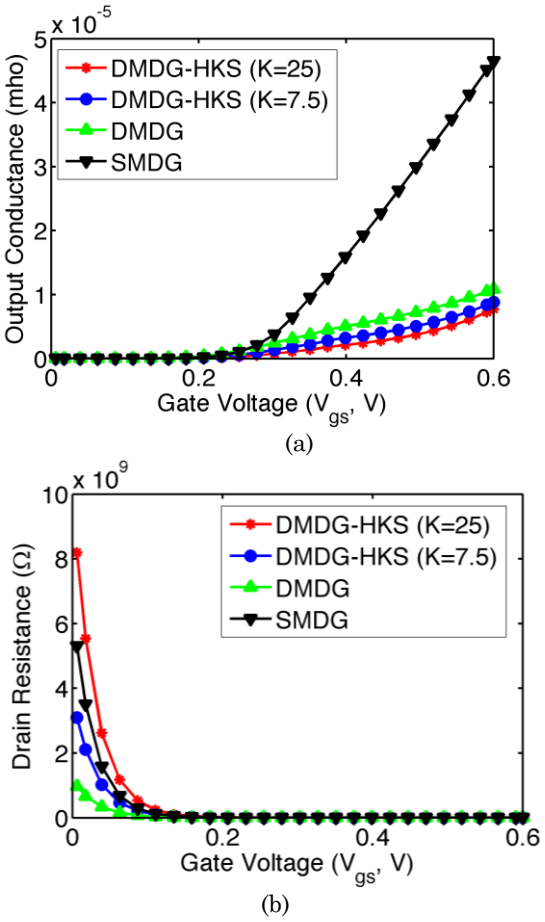


Fig. 6 – Comparison of drain conductance (a) and resistance of different structures at $V_{DS} = 0.6$ V (b)

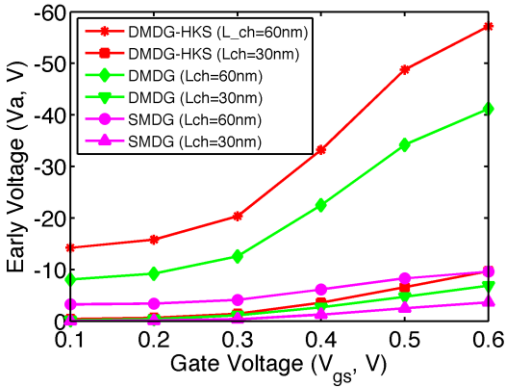


Fig. 7 – Comparison of early voltage V_a between different structures at $V_{DS} = 0.6$ V

(Fig. 6b) is highest for the DMDG-HKS ($K = 25$) and is lowest for the SMDG for small values of V_{GS}. This indicates a decrement in the OFF state leakage current.

Fig. 7 shows the early voltage (V_a) of different structures. The early voltage is highest for the DMDG-HKS MOSFET ($K = 25$) in the DIBL dominated region (i.e. when V_{DS} is high). This is due to the reasons that (i) the device is highly immuned to drain bias variations by virtue of DMG architecture and (ii) enhanced gate controllability on the channel charge with reduced EOT offered by high-k stack [14]. The large value of early voltage signifies a weak dependence of the transistor current on the drain to source voltage (V_{DS}). At higher gate voltages, the gate exerts a relatively larger influence on the field lines which, in turn, weakens the influence of the drain. Thus early voltage is higher in strong inversion than in weak inversion [16].

Fig. 8 represents the intrinsic gain (A_v, g_m / g_d) being expressed in decibels (dB). It can be observed that the intrinsic gain in the subthreshold regime of operation is higher due to an exponential behavior of the drain current in this regime giving rise to a larger TGF [12]. We can see that the DM gate MOSFETs have higher intrinsic gain than SMDG. The improvement is further enhanced in case of gate oxide stacks i.e. DMDG-HKS. The superior TGF and low drain conductance (g_d) of DMDG-HKS serves to provide higher gain than DMDG or SMDG.

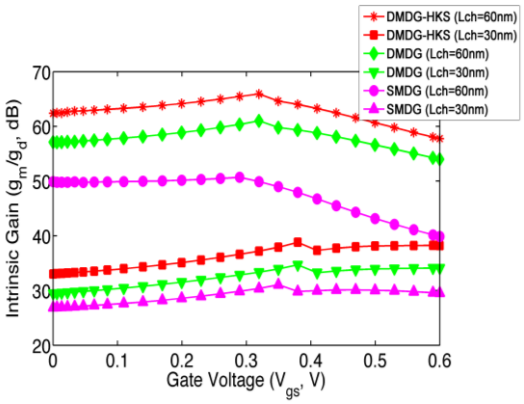


Fig. 8 – comparison of intrinsic gain (dB) between different structures at $V_{DS} = 0.6$ V

3.3 RF Performance

The intrinsic gate capacitance is an important parameter in RF analysis. Here, all the capacitances have been extracted from small signal ac device simulations at an operating frequency of 1 MHz. DMDG-HKS has larger gate capacitance compared to the other configurations due to the less EOT as shown in Fig. 9a. The gate capacitance per unit area in terms of equivalent oxide thickness, EOT defined by (1), is given by

$$C_{gg} = \frac{\varepsilon_{SiO_2}}{EOT} \qquad (3)$$

Indeed total gate capacitance is due to the gate to channel capacitance plus gate to source / drain capacitance (fringing capacitance). If we use the high-k dielectric material alone as gate oxide then the EOT will be less for high-k gate oxide as compared to the SiO_2 ($\varepsilon_{high\text{-}k} > \varepsilon_{SiO_2}$) for the same physical thickness of the oxides; hence the gate capacitance is also higher for high-k as compared to the SiO_2. If we make the EOT of high-k same as SiO_2, the physical thickness of the high-k has to be increased in proportion (($\varepsilon_{high\text{-}k} / \varepsilon_{SiO_2}$) times) and a thicker gate oxide will lead a lot more fringing fields from its side walls to be mapped on the source / drain regions, thereby increasing the fringing capacitances. Hence the overall gate capacitance will be increased.

The above conclusion can be verified from the plots in Fig. 9b in which the solid lines represent MOSFETs with same oxide physical thickness (2 nm) and the dotted lines represent MOSFETs with same EOT (1 nm, for HfO_2 with $K = 25$, $t_{ox} = 6.41$ nm and for Si_3N_4 with $K = 7.5$, $t_{ox} = 1.92$ nm) keeping other device parameters identical – gate length 30 nm (for DMDG-HKS, 15 nm (M1, 4.6 eV) + 15 nm (M2, 4.1 eV)), channel doping 1E + 16 cm^{-3}, source / drain doping 1E + 20 cm^{-3}.

It can be observed that the gate capacitance is larger for the MOSFET with higher K value with the same values of EOTs due to larger fringing capacitance resulting from gate oxides of higher K value (thicker gate oxide). Also, the EOT of DMDG-HKS is smaller as compared to other two MOSFETs (i.e. DMDG and SMDG) resulting in an increased total gate capacitance.

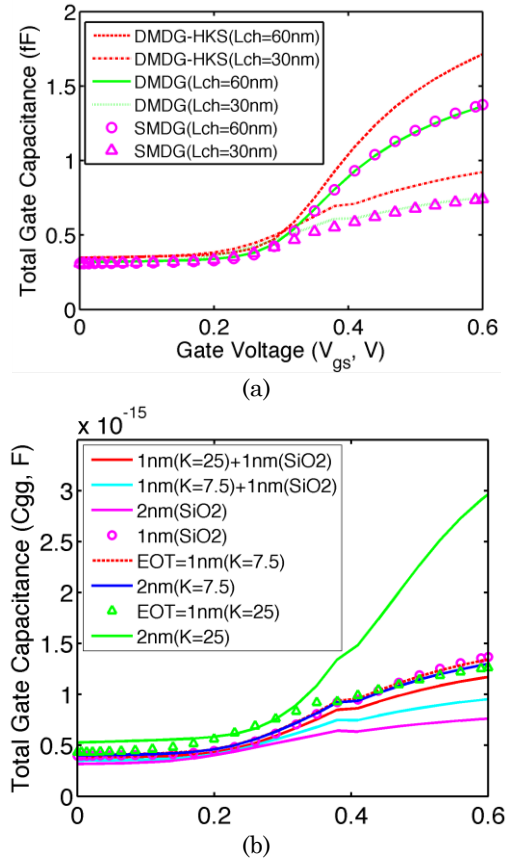


Fig. 9 – Comparison of total gate capacitance (a) different structures with same physical thickness of 2 nm (b) different structures with same physical thickness (solid line) and same EOT (dotted line / symbols) at frequency of 1 MHZ as a function of V_{GS} with $V_{DS} = 0.6$ V

Next, we consider the transition frequency (f_T), defined as the frequency at which the magnitude of the short circuit current gain decreases to 1, and is given by [15, 28]

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (4)$$

Where C_{gg} is the total gate.

For f_T extraction, a mixed mode environment is set up for AC simulation in Sentaurus Device of Sentaurus TCAD. Here, a two-port network circuit configuration is used in which voltage sources are attached to the gate (port 1) and drain (port 2) terminals and all other terminals are grounded [17]. The AC analysis is performed over a frequency range and the *Y*, *Z* and *H* parameters are computed from which f_T is extracted using unity-gain-point method of inspect tool.

In Fig. 10, DMDG-HKS ($K = 25$) shows slight reduction of f_T values when compared with that of DMDG. This is because of the decrease of EOT of gate oxide with the use of high-k dielectric, resulting in an increase of total input gate capacitance which degrades the f_T values. Whereas the intrinsic gain g_m / g_d still increases because of the enhanced g_m, reduced g_d increased V_a, and suppressed SCEs [14]. With the increase of permittivity, C_{gg} increases but the increase in g_m is not sufficient to compensate the increase in gate capacitance, thereby decreasing f_T as compared to DMDG. But DMDG-HKS ($K = 25$) has higher f_T than SMDG even though the gate capacitance for the first is higher. It is because of g_m of the DMDG-HKS ($K = 25$) which is much greater than the SMDG and hence is able to compensate the increase in C_{gg} thereby providing a higher value of f_T.

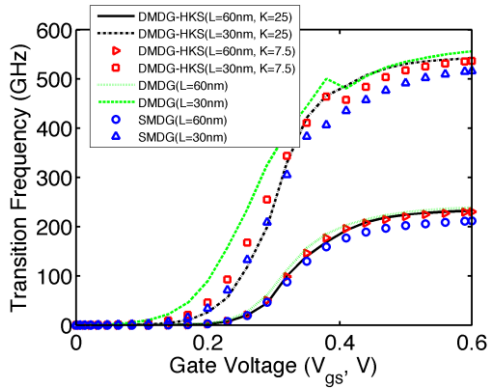


Fig. 10 – Comparison of transition frequency for different structures using unity gain method

3.4 Effect of Gate Length Scaling on Analog and RF Performance

For assessing the effect of gate length scaling on the analog and RF performance of DMDG-HKS MOSFETs, we have considered the following device parameters – gate oxide comprising of 1 nm SiO_2 + 1 nm high-k (HfO_2) stack, gate metals of height 2 nm with work functions 4.6 eV (M1) and 4.1 eV (M2), source / drain doping 1.0×10^{20} cm^{-3}, channel doping 1.0×10^{16} cm^{-3}, and body thickness 10 nm.

The drain conductance (Fig. 11a) increases and output resistance (Fig. 11b) decreases with the decrease of gate length. Transconductance increases while the TGF decreases with decrease in channel length as observed in Fig. 12a and b, respectively.

The early voltage V_a, (Fig. 13) of the DMDG-HKS increases with the increase of gate length. This is due to the reduced effect of the drain voltage on the channel under gate M1. As the gate length decreases the drains affects the channel charge and for very small gate lengths it becomes sever and the metal gate M2 is not able to screen the drain field effect.

Fig. 14 shows a decrease in intrinsic gain (g_m / g_d) with gate length. This is due to the reason that the transconductance does not increases as much with the decrease in length as does the output conductance.

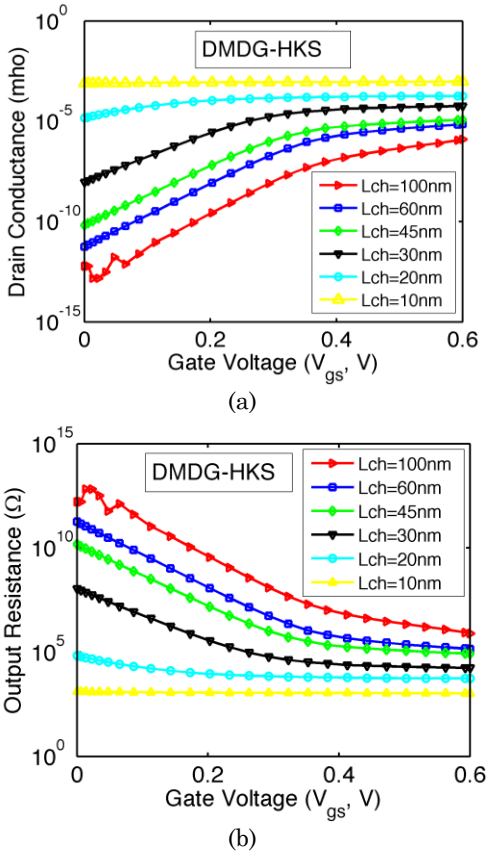
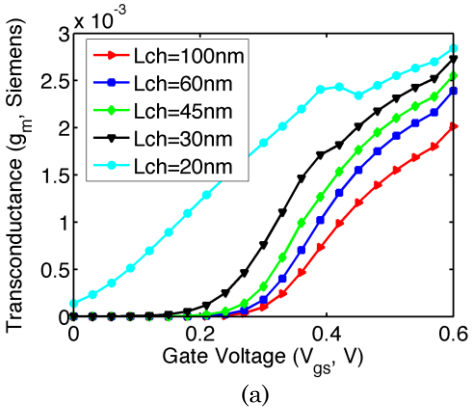
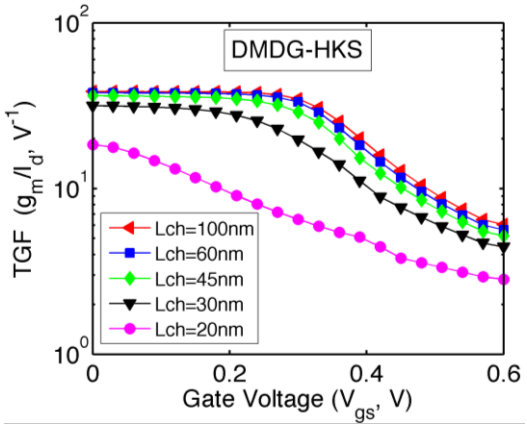


Fig. 11 – Drain (a) conductance and (b) output resistance of DMDG-HKS structure for different gate lengths





(b)

Fig. 12 – Comparison of (a) transconductance and (b) TGF of DMDG-HKS structure for different gate lengths at V_{DS} = 0.6 V

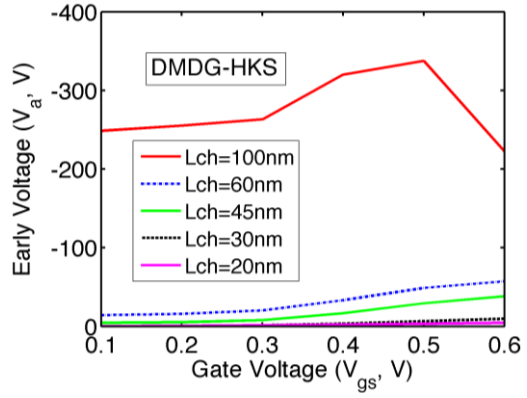


Fig. 13 – Comparison of early voltage for different gate lengths

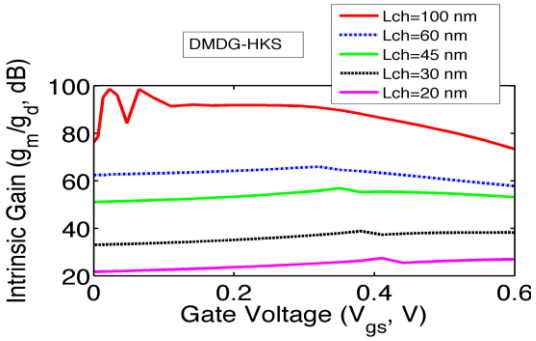


Fig. 14 – Comparison of Intrinsic gain for different gate lengths of DMDG-HKS at V_{DS} = 0.6 V and operating frequency 1 MHz

The gate capacitance as shown in Fig. 15 increases with the increase of gate length since the total gate area increases. The transition frequency which depends on the ratio of transconductance and gate capacitance, decreases with the increase of gate length as observed in the Fig. 15. This is due to the reason transconductance is lower for larger gate length and gate capacitance is larger due to larger gate area.

Transition frequency variation is compared and shown in Fig. 16 for various gate lengths of the DMDG-HKS MOSFETs and is found to be highest for the lowest gate length. The maximum frequency of oscillation as in Fig. 17 is good for the largest gate length.

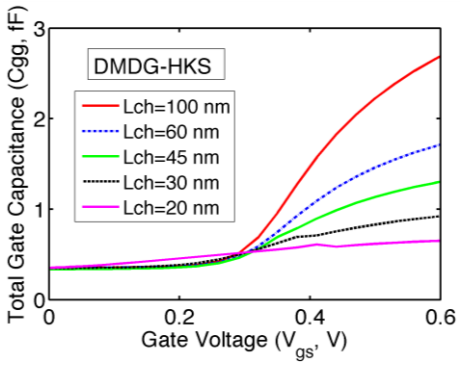


Fig. 15 – Total gate capacitance for different gate lengths of SMDG-HKS at V_{DS} = 0.6 V and operating frequency 1 MHz

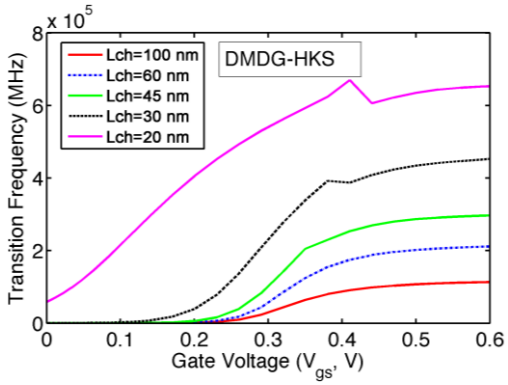


Fig. 16 – Transition frequency variations of DMDG-HKS MOSFETs

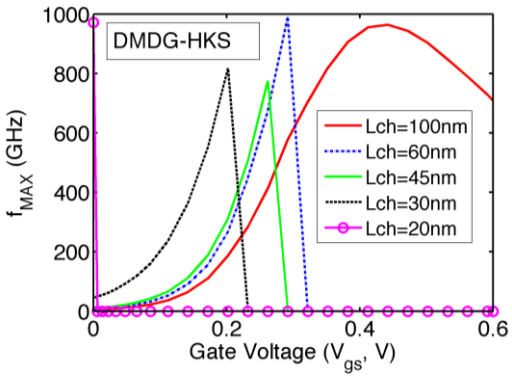


Fig. 17 – Maximum frequency of oscillation

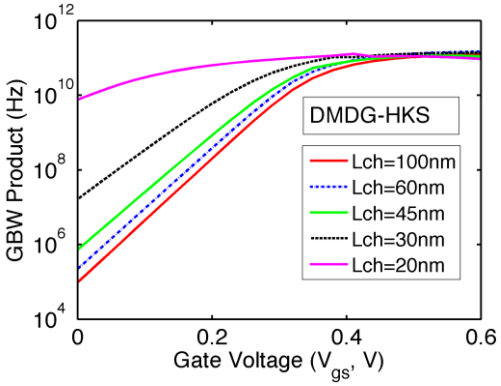


Fig. 18 – Comparison of Gain Band Width (GBW) product

4. CONCLUSIONS

In this paper, we have investigated the short channel effects and analog/RF performance of the DMDG-HKS MOSFETs with different values of high-k. It was found that DMDG-HKS stack has a better control of channel region by the gate than the DMDG and SMDG MOSFETs. Due to this, it has better current characteristics and SCE control. Improvements in analog performance were observed in terms of transconductance, transconductance generation factor, early voltage, reduced drain conductance, and higher intrinsic gain. Transition frequency of DMDG-HKS shows slight degradation with the increasing values of high-k due to the increase in the total gate capacitance as compared to DMDG but it is still greater than that of the SMDG MOSETs. Various analog and RF parameters have been observed by varying the gate length of DMDG-HKS MOSFETs. The transition frequency has been observed to be decreasing with the increase in gate length of DMDG-HKS MOSFETs. Other parameters like TGF, early voltage, intrinsic gain, and gate capacitance scale with gate length whereas there is a slight increase of transconductance.

Fig. 18 shows the gain band width (GBW) product which is computed by the approximate formula given by

$$GBW = \frac{g_m}{2\pi.10.C_{gd}} \quad (5)$$

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REFERENCES

1. Anurag Chaudhary, M. Jagadesh Kumar, *IEEE T. Dev. Mat. Rel.* **4**, 99 (2004).
2. Jean-Pierre Colinge, *Solid-State Electron.* **48**, 897 (2004).
3. Qiang Chen, Keith A. Bowman, Evans M. Harrell, James D. Meindl, *IEEE Cir. Dev. Magazine* 28 (2003).
4. Wei Long, Haijiang Ou, Jen-Minkuo, Ken K. Chin, *IEEE T. Electron Dev.* **46**, 865 (1999).
5. A.K. Kushwaha, *Phd thesis* (NIT Kuruksetra: India: 2011).
6. Anurag Chaudhry, M. Jagadesh Kumar, *IEEE T. Electron Dev.* **51**, 1463 (2004).
7. Hisayo Sasaki Momose, Tatsuya Ohguro, Kenji Kojima, Shinichi Nakamura, Yoshiaki Toyoshima, *IEEE T. Electron Dev.* **50**, 1001 (2003).
8. A.P. Haung, Z.C. Yang, Paul K. Chu, *Advances in Solid State Circuits Technologies* (Croatia: INTECH: 2010).
9. G.C.F. Yeap, S. Krishnan, Ming Ren Lin, *Electron. Lett.* **34**, 1150 (1998).
10. Pedram Razavi, Ali A. Orouji, *11th International Biennial Baltic Electronics Conference* (BEC2008), 83 (Tallinn: Estonia: 2008).
11. N. Mohankumar, Binit Syamal, C.K. Sarkar, *IEEE T. Electron Dev.* **57**, 820 (2010).
12. Saurav Chakraborty, A. Mallik, C.K. Sarkar, *IEEE T. Electron Dev.* **55**, 827 (2008).
13. *Sentaurus TCAD user's Manual* (2009).
14. Poonam Kasturi, Manoj Saxena, Mridula Gupta, R.S. Gupta, *IEEE T. Electron Dev.* **55**, 382 (2008).
15. N. Mohankumar, Binit Syamal, C.K. Sarkar, *Microelectron. Rel.* **49**, 1491 (2009).
16. Amara Amara, Olivier Rozeau, *Planar Double-Gate Transistor: From Technology to Circuit* (Springer: 2009).
17. Y. Tsividis, *Operation and Modeling of MOS Transistor* (New York: McGrawHill: 1999).
18. P. Ranade, et al., *IEDM Tech. Dig.* 217 (2005).
19. L. Ragnarsson, et al., *IEDM Tech. Dig.* 663 (2009).
20. Takashi Matsukawa, et. al., *IEEE Electr. Device L.* **29**, 618 (2008).
21. Tzung-Lin Li, Wu-Lin Ho, Hung-Bin Chen, Howard C.-H. Wang, Chun-Yen Chang, Chenming Hu, *IEEE T. Electron Dev.* **53**, 1420 (2006).
22. F. Arnaud, et al., *IEDM Tech. Dig.* 633 (2008).
23. T. Tomimatsu, et al., *VLSI Tech. Dig.* 36 (2009).
24. K. Choi, et al., *VLSI Tech. Dig.* 138 (2009).
25. C. Lai, et al., *IEDM Tech. Dig.* 655 (2009).
26. M.A. Pavanello, J.A. Martino, V. Dessard, D. Flandre, *Electrochem. Solid-State Lett.* **3**, 50 (2000).
27. M. Shur, *Appl. Phys. Lett.* **54**, 162 (1989).
28. Onur Esame, Yasar Gurbuz, Ibrahim Tekin, Ayhan Bozkurt, *Microelectr. J.* **35**, 901 (2004).
29. *Sentaurus Technology Template: DC and RF Characterization of HEMTs* (2007).
30. *Inspect Users Guide, Sentaurus TCAD* (Synopsys: 2007).
31. Qiang Lu, Yee Chia Yeo, Pushkar Ranade, et al., *Symp. on VLSI Tech. Digest of Tech. Pap.* (2000).
32. Igor Polishchuk, Pushkar Ranade, Tsu-Jae King, Chenming Hu, *IEEE Electr. Device L.* **23**, 200 (2002)
33. Veena Misra, Huicai Zhong, Heather Lazar, *IEEE Electr. Device L.* **23**, 354 (2002).
34. J.H. Sim, H.C. Wen, J.P. Lu, D.L. Kwong, *IEEE Electr. Device L.* **24**, 631 (2003).
35. W.P. Maszara, *J. Electrochem. Soc.* **152**, G550 (2005).